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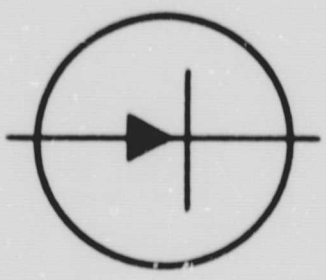

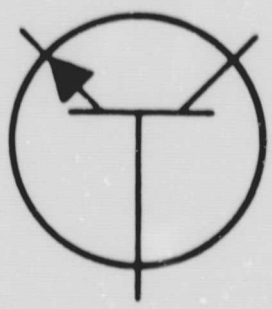

WESTINGHOUSE ELECTRIC CORPORATION
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Interim Summary Report - Mod. 2

Development of Multilayer Epitaxy for High Reliability Transistors

April 1968 through December 1968

CONTRACT NO. NAS8-18125
DCN 1-6-40-68627 (1F)

National Aeronautics and Space Administration
George C. Marshall Space Flight Center
Huntsville, Alabama 35812

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ABSTRACT

This report describes the design and process technology developed to yield high reliability, high current transistors. These 100-ampere PNP transistors have epitaxially grown base and collector regions, diffused emitter regions, and feature compression bonded encapsulation. Transistors with several different collector resistivities and base widths were investigated to determine the relationship between high current h_{FE}, $V_{CE(sat)}$ and $V_{CEO(sus)}$. In order to improve the gain and saturation performance for a given sustaining voltage, methods of increasing bulk lifetime were evaluated.

1. INTRODUCTION

The development of a multiple epitaxial transistor was initiated under a previous contract, NAS8-5335, supported by the NASA Astrionic Laboratories, Marshall Space Flight Center, Huntsville, Alabama. Under that contract the multiple epitaxial design achieved the equivalent of a 100% wafer yield by the successful development of a high speed NPN power transistor approximately one inch in diameter. In a subsequent contract, NAS8-18125, the correlation between design parameters and secondary breakdown was established. A family of fast switching NPN power transistors incorporating the multiple epitaxial approach was introduced commercially by Westinghouse.

Continuing under NAS8-18125, a PNP transistor employing the multiple epitaxial concept was developed to complement the fast switching NPN devices. The salient characteristics of the PNP devices are:

$V_{CEO(sus)}$	=	150 volts
f_T	=	30 MHz
Total Switching	<	1 μs
$I_{C(max)}$	=	30 amperes

In addition, excellent secondary breakdown performance was demonstrated.

The present study concerns the extension of the PNP multiple epitaxial technology to the development of high current PNP transistors employing a circular geometry approximately one inch in diameter to yield a 100-ampere device.

A. DEVELOPMENTAL SEQUENCE

For this study a circular geometry ~ 1" in diameter with 24" of emitter edge length was used. This geometry is shown in Figure 1. The initial design objective specifications are shown in Table 1. The ambitious objectives require obtaining the necessary 100-ampere h_{FE} and saturation voltage, while retaining the 150-volt sustaining voltage. In general the available trade-offs are such that the physical parameter changes that increase $V_{CEO(sus)}$ also increase $V_{CE(sat)}$ and $V_{BE(sat)}$ and decrease high current gain. The experimental approach in this study was to first determine the parameters necessary to obtain 150-volt $V_{CEO(sus)}$ and then to improve the gain and saturation performance, primarily by increasing lifetime. Increasing the lifetime for holes in the base region improves gain for a transistor by increasing the base transport factor. This lifetime results in a longer diffusion length, L_{pb}, where $L_{pb} = \sqrt{D_{pb}\ \tau_{pb}}$. D_{pb}, the diffusion constant for holes in the base, is fixed for a given resistivity. It is seen that increasing τ_{pb} results in improved current gain because the longer diffusion length means more holes reach the collector of the transistor and fewer are lost by recombination with electrons. Improved gain also results in lower saturation voltage. The most successful method of improving lifetime was found to be a P_2O_5 gettering operation after emitter diffusion. Process details are discussed in a later section.

B. MAJOR ACCOMPLISHMENTS

The use of a multiple-epitaxial technique in fabricating large area fast switching PNP silicon power transistors has been demonstrated. The design and process showed a capability of producing transistors with usable gain at collector currents of 100 amperes, sustaining voltages greater than 200 volts, total switching time of less than 2 microseconds, and f_t's of approximately 10 MHz. A monolithic, 100-ampere, 200-volt,

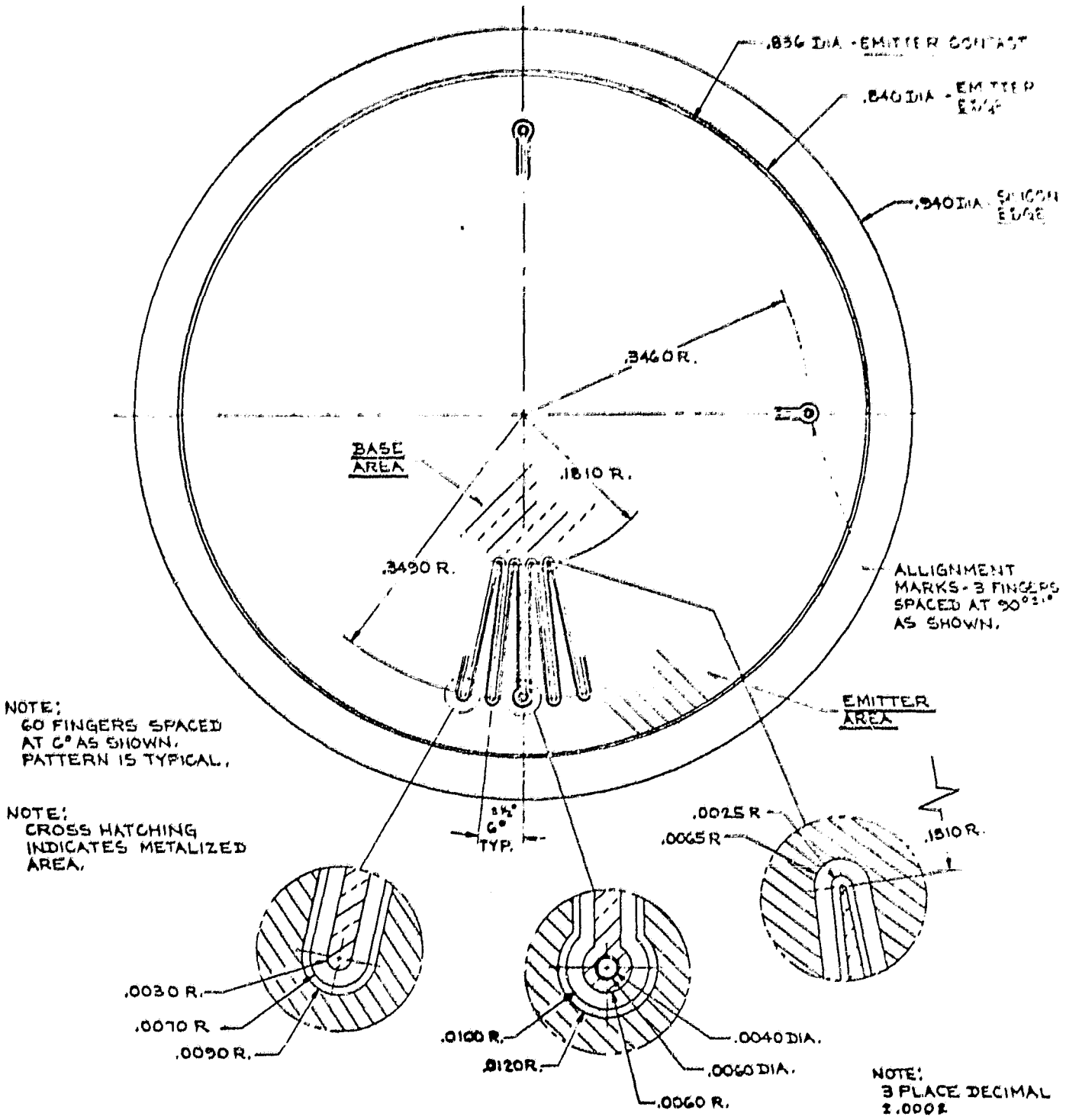


Figure 1. Transistor Geometry

Table 1

DESIGN OBJECTIVE SPECIFICATIONS

1. $V_{CEO(sus)} = 150V$

2. $h_{FE} = 15 @ I_C = 100A$

3. $V_{CE(sat)} = 1V @ I_C = 100A$

4. $V_{BE(sat)} = 1.8V @ I_C = 100A$

5. Determine switching speed and frequency response

fast switching PNP transistor represents a significant advance in the state-of-the-art. The inherent advantage of the epitaxial base technique over other fast switching transistor processes involving base diffusions and superiority of the compression bonded encapsulation techniques are of paramount importance to this development.

The electrical characteristics demonstrate the trade-offs available between $V_{CEO(sus)}$, h_{FE} and $V_{CE(sat)}$. This knowledge permits fabrication of transistors tailored for specific circuit applications.

2. MATERIAL PREPARATION

A. BACKGROUND

The basic equipment and process technique for growth of epitaxial silicon as well as the method of evaluation have been described in detail previously (Final Report on Contract No. NAS8-18125, DCN 1-6-40-6827(1F), July 1966 through March 1967). However, the sequential operation and parameters have been modified for the present PNP transistor.

B. EPITAXIAL PROCEDURE

The epitaxial procedure for the 30 and 100-ampere device consists of heating the substrates to 1200°C in a filtered dry hydrogen atmosphere. Pure gaseous HCl is introduced to etch the substrates prior to growth. The reaction of HCl and silicon is the reverse of the deposition reaction and permits the removal of the environmental work damage caused by chemical polishing.

$$4HCl + Si \longrightarrow SiCl_4 + 2H_2$$

Sufficient silicon is removed to insure a lattice match for the growth operation.

The HCl procedure is followed with a pure hydrogen treatment at 1200°C to clean out the reaction area of any chlorides which could act as nucleation sites. A layer of P-type conductivity is deposited to the required resistivity and thickness. The N-type layer is then deposited in situ to the desired thickness and the resistivity is controlled with phosphine gas as the dopant. After the N deposition, the system is purged with pure hydrogen to remove the dopant and halide traces. The system is then cooled for the removal of the silicon wafers.

C. MATERIAL REQUIREMENTS

Crystal specifications:

- P-type
- Resistivity: .008-.01 ohm-cm
- Radial resistivity gradient: 15% (max.)
- Diameter: 1.3" $\pm$ .001"
- Dislocation density: 0-200/cm^2
- Orientation: within 2° of the (111)
- Lifetime: as high as possible
- Lineage: none
- Other imperfections: none

D. EPITAXIAL EVALUATION

The epitaxial layers are evaluated by conventional sectioning techniques to measure the thickness of the epi P-type and N-type regions. The wafers are examined visually to detect any gross crystalline defects. Spreading resistance measurements are made on a sample basis primarily to determine the resistivity of the P^- epitaxial region, since conventional staining techniques do not readily provide this information. Figure 2 is a typical spreading resistance plot made on an epitaxial run. The plot is shown as it is recorded. A correction should be made for points recorded near a junction. This correction is made with the use of a computer program and is such that the N-type base region is of a more uniform resistivity than the raw data indicate.

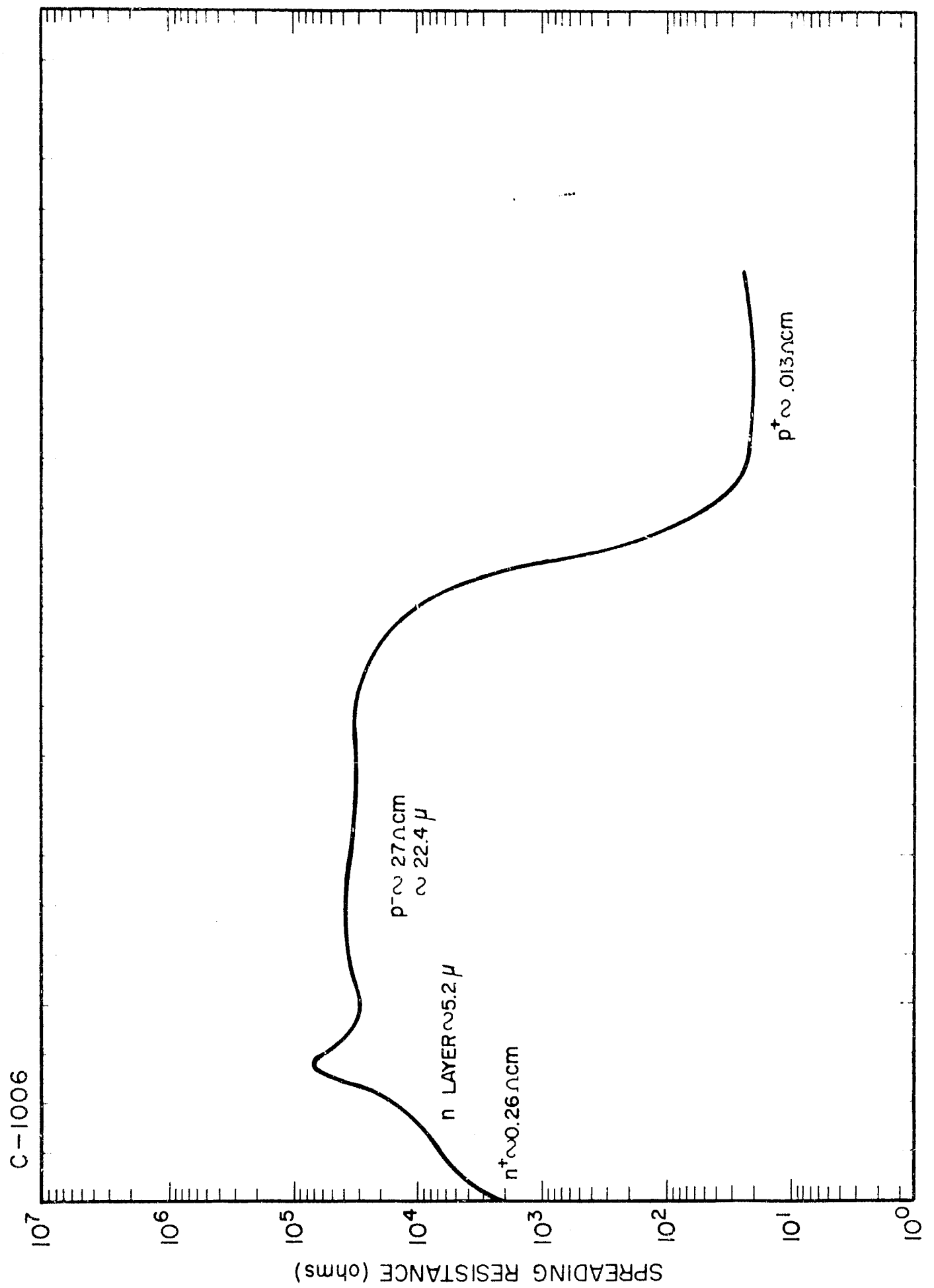


Figure 2. Spreading Resistance Profile

3. FABRICATION PROCESSES

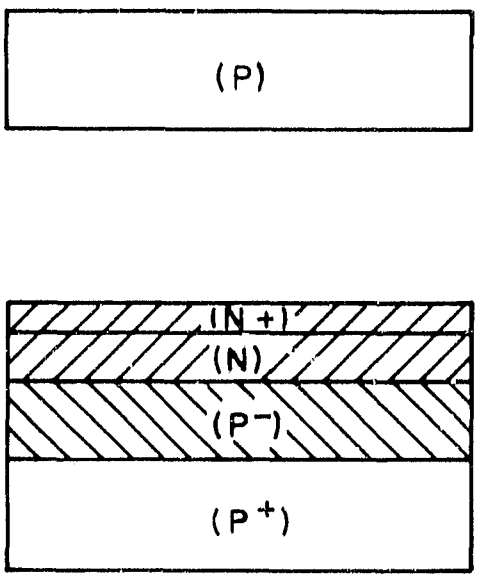
A. PROCESS FLOW

Figure 3 is a flow chart showing schematically the process sequence. Prior to all diffusion operations, the silicon wafers are subjected to a thorough pre-diffusion cleaning. This consists of soaking the wafers alternately in hot sulfuric acid, hot nitric acid and hot filtered deionized water. Immediately prior to the actual diffusion operation, the wafers are blown dry with filtered nitrogen and placed on the quartz diffusion boat. This is done in a dust-free atmosphere. All diffusion operations are performed with the wafers lying horizontally on the diffusion boat. Placing the wafers vertically increases capacity, but it results in induced crystal imperfections as demonstrated in the earlier phases of this contract.

All photomasking operations utilize conventional techniques. Commercially available KMER is used for all masking operations. It is applied, cured, exposed and developed using well-known techniques. After etching, the KMER is removed using hot sulfuric acid or hot trichloroethylene. The trichloroethylene must be used in those operations where aluminum metal is present on the wafer.

B. OXIDATION

The first process step after epitaxial growth is the initial oxidation. The purpose of this operation is to provide an SiO_2 layer thick enough to mask against the subsequent emitter diffusion. The wafers are oxidized for 40 minutes at 1100°C in an atmosphere of $H_2O_{(g)}$ to produce an SiO_2 layer > 3000Å thick.



STARTING MATERIAL

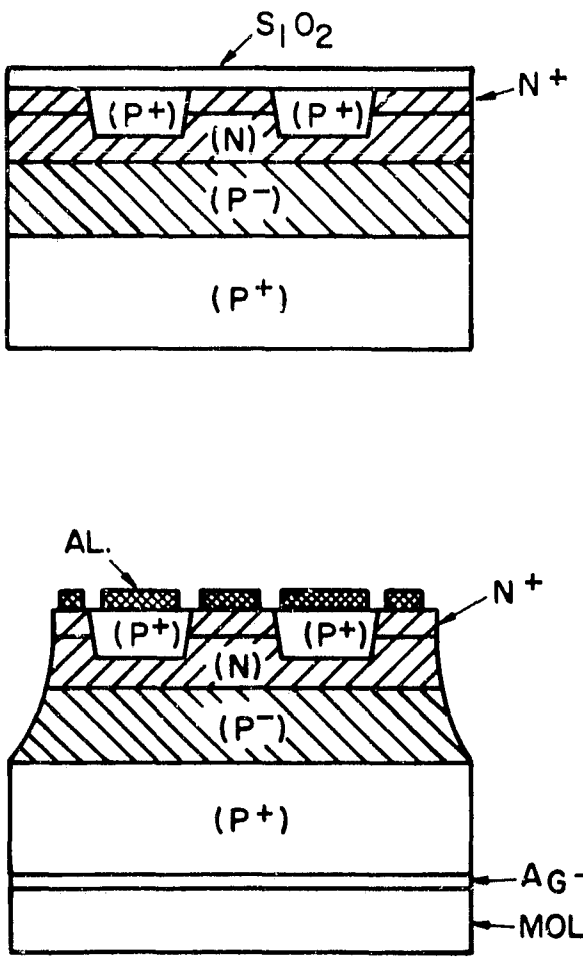
.01Ω CM P TYPE, B DOPED
CHEMICALLY POLISHED
6-7 MILS THICK

EPITAXIAL GROWTH

P^- 20U 10-25ΩCM
N 5U 0.5-1.0ΩCM
N^+ 0.3U 0.01ΩCM

OXIDATION

OXIDATION-1100°C 30MIN.



EMITTER MASKING & DIFFUSION

B_2H_6 DEPOSITION-1150°C 15MIN.
OXIDATION-1100°C 11MIN.
P^+ P = 6×10^{19} ATOMS/CC X_J = 0.9U-3.3U
W_B = 1.2U TO 4.5U

CONTACT MASKING, METALLIZATION & JUNCTION ETCHING

AL. EVAPORATION 40,000 A°

Figure 3. Process Flow Chart

C. SANDBLASTING

The starting Si wafer diameter is 1.3". The purpose of the sandblasting operation is to reduce the diameter to 0.94". This is done prior to emitter photomasking to maintain the radial symmetry of the device geometry. The initial 1.3" diameter was chosen to improve epitaxial wafer uniformity, as it is well known that variations within epitaxial layers are pronounced near the edge of a wafer due to variations in reactant gas flows at the wafer-gas stream interface. After sandblasting the Si surface at the perimeter is damaged, but the damage will later be removed by Si etching. The sandblasting operation is done after oxidation so that the SiO_2 protects the Si surfaces from contamination.

D. EMITTER MASKING AND DIFFUSION

After sandblasting the wafers are ready for emitter photomasking to define the emitter geometry on the wafer. Oxide is removed from those areas where diffusion is desired. It is left on those areas where diffusion is not desired.

The emitter diffusion is done at 1150°C in an atmosphere of $B_2H_{6(g)}$, $O_{2(g)}$ and $N_{2(g)}$. The time is determined by the thickness of the epitaxial base region and the desired base width. The diborane system was used instead of a boron tribromide system because of the desirability of high surface concentration that is more readily attainable with diborane. The problem with this boron diffusion is to obtain the high concentration while avoiding the formation of an insoluble boron glass which would prevent further masking steps. Diborane proved superior to tribromide in this respect. The 6×10^{19} atoms/cc concentration reported for this study represents the maximum Co that could be obtained reproducibly without the formation of an insoluble boron glass.

After the emitter diffusion, the wafers are oxidized at 1100°C in an atmosphere of $H_2O_{(g)}$ and $O_{2(g)}$. This serves to dilute the boron-doped

oxide formed during emitter diffusion and facilitate the subsequent contact photomasking operation. The oxidation step does not appreciably affect the base width (W_B) which is determined by the 1150°C B_2H_6 diffusion.

E. GETTERING

One method of improving the high current gain of epi base PNP transistors is to increase the lifetime of holes in the base region since this will increase the base transport factor. The most successful method found to improve the lifetime of the subject transistor was a P_2O_5 gettering step after emitter diffusion. The gettering is done for 15 minutes at 950°C in a two-zone diffusion furnace with the P_2O_5 source at 300°C. After diffusion the P_2O_5 source is removed and the wafers are removed from the 950° zone over a 15-minute interval to approximate a slow cool.

It was discovered experimentally that the oxide grown during emitter diffusion is not thick enough to be an effective mask against the P_2O_5 diffusion. Since a high temperature oxidation would affect the base width a low temperature (650°C) oxide deposition from the reaction

$$SiH_{4(g)} + 2O_{2(g)} \dashrightarrow SiO_{2(s)} + 2H_2O_{(g)}$$

was utilized to obtain the necessary thickness of SiO_2. After SiO_2 deposition the oxide is selectively removed from the collector surface. After gettering all the oxide is removed and a new SiO_2 layer is deposited for the contact photomasking to protect the emitter base junction and to insure alignment after Al evaporation. The collector surface is given a brief Si etch to remove the N^+ layer formed during gettering.

One method of measuring the effectiveness of the gettering is to measure the lifetime before and after gettering. A diode recovery

type evaluation indicated 1.5 microseconds before gettering and 3.2 microseconds after gettering. Actual device measurement indicated improved gain and saturation performance.

F. METALLIZATION

After oxide deposition the wafers are ready for contact photomasking, which serves to remove the oxide from the emitter and base contact areas where ohmic contact will be made using Al. This is done prior to molybdenum mounting, thereby eliminating the need to protect the molybdenum from attack by the oxide etching solution.

Initially the wafers were soldered to the Mo using a Pb-Ag-Sb solder in a vacuum RF system. Since the possibility of the Sb forming an N-type junction exists later runs were made with a lower melting Al-B solder.

Aluminum is evaporated using a conventional filament evaporator, except that the wafers are heated to 500°C in vacuum prior to evaporation. This is done to insure surface cleanliness. The evaporated layer is ~40,000Å thick.

Inverse contact photomasking serves to define the emitter and base contact areas after which wafers are heated to 570°C for 1 min. to alloy the Al to form ohmic contacts.

G. JUNCTION PREPARATION

It is necessary to etch the collector-base junction to develop the collector-base and the collector-emitter voltages. The etch is necessary to remove the surface damage caused by the initial sandblasting operation and to remove the unwanted P-type diffused region formed during emitter diffusion. Essentially this operation consists of two steps. The first step involves a gross removal of Si and serves to

define the junction angle. This is either done by sandblasting or by a beveling step where the Si is removed by a polishing wheel. The second step is a junction etching. This is done in a spin etching machine where a stream of Si etch solution is directed at the sand-blasted or beveled C-B junction, while the fusion is rotating on a spindle. The rotation keeps the Si etch solution from the metallized surfaces of the device. After etching, the devices are immediately rinsed with water within the spin etch machine.

After etching the transistor is ready for initial electrical evaluation. Low current h_{FE}, BV_{CBO}, BV_{CEO}, and BV_{EBO} are tested. Units that pass electrical evaluation are sent for junction coating. The exposed C-B junction is coated with a silicone-alizarin mixture and cured 16 hours at 240°C. This coating serves to passivate and to protect the collector base junction.

H. ENCAPSULATION

The details of the compression bonded encapsulation technique are discussed in detail in an earlier report[1]. Figure 4 shows a schematic representation of an encapsulated device.

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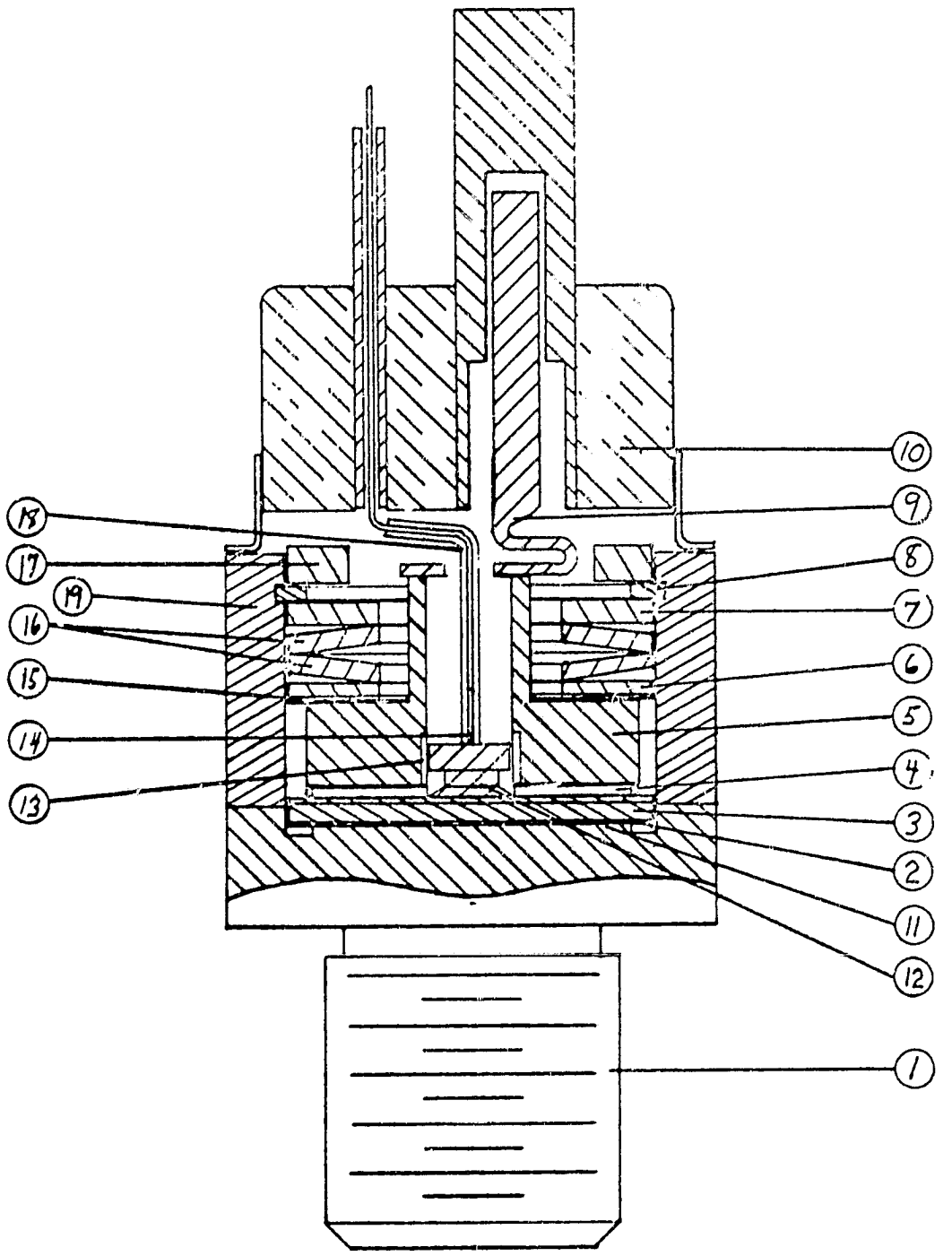
(1) Final Report, "Development of Multilayer Epitaxy for High Reliability Transistors," July 1966 through March 1967, Contract NAS8-18125, DCN 1-6-40-68627(1F).



1. base
2. silver foil
3. basic transistor
4. emitter contact
5. emitter lead
6. flat washer
7. flat washer
8. retaining ring
9. silver emitter lead
10. ceramic-metal seal
11. silver pedestal
12. base contact
13. Teflon insulation
14. base lead wire
15. mica insulation
16. Belleville springs
17. molecular sieve
18. base lead insulation
19. integral case

Figure 4. Components of 100-Amp Encapsulation

4. TESTING AND ELECTRICAL RESULTS

A. ELECTRICAL TESTING

A Dynatran, Model 2158, pulsed curve tracer is used for the measurement of high current gain, $V_{CE(sat)}$, and $V_{BE(sat)}$. This equipment operates on a 1% duty cycle with a triangular collector pulse of 150 microseconds. The base supply is on for 300 microseconds with the collector pulse centered within this time period.

I_{CEO}, I_{CBO}, and I_{EBO} are measured on a Tektronix, Model 575, curve tracer. $V_{CEO(sus)}$ is measured on the circuit shown schematically in Figure 5. This test set will sweep the transistor under test through an inductive load line to obtain the sustaining characteristics of the collector-emitter junction. In operation, a modest current is passed through the transistor with an inductor in series with the collector. The transistor is then turned off very rapidly and the industor is discharged through the collector-emitter circuit. The discharge of this inductor will sweep the collector to a high voltage at approximately constant collector current until breakdown of the collector-emitter junction occurs in the sustaining mask. The sustaining characteristics are determined by observing this load line on an oscilloscope and reading the maximum voltage at the specified current.

The f_t tester uses one-quarter wavelength transmission lines for isolation of the power supplies and also for the short circuit load. When a quarter wavelength of transmission line (cut to the selected frequency) is shorted on one end with a capacitor, the other end approaches an infinite input impedance. This high impedance end is connected to the transistor and the collector and base bias supplies are isolated from the RF. A quarter wavelength transmission line is connected to the collector-emitter terminals with a high impedance RF voltmeter connected

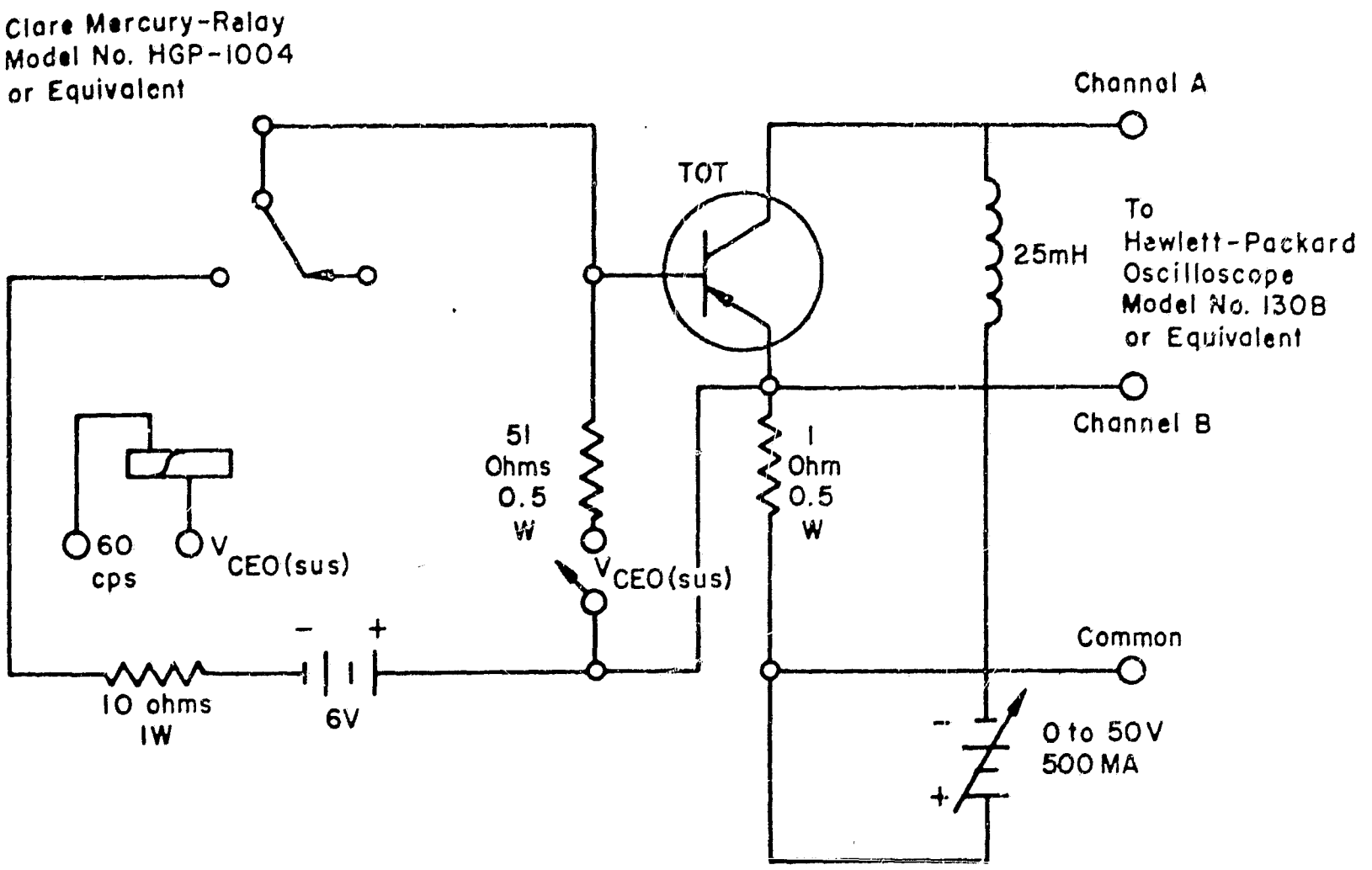


Figure 5. Schematic - Sustaining Voltage Tester

to the other end of this transmission line. Since a quarter wavelength transmission line acts as an impedance transformer, the collector-emitter is essentially short-circuited to RF current. An input RF voltage is applied to the base and the base RF current is measured. The output RF current, using transmission line theory, is $i_{out} = E_{out}/Z_o$ where E_{out} is the RF output current and Z_o is the characteristic impedance of the transmission line. Therefore, $h_{FE} = i_o/i_{in}$ where i_o = output RF current and i_{in} = input RF current. The gain-bandwidth product f_t = frequency of measurement multiplied by h_{FE} when the frequency of measurements is on the 6 db/octave slope.

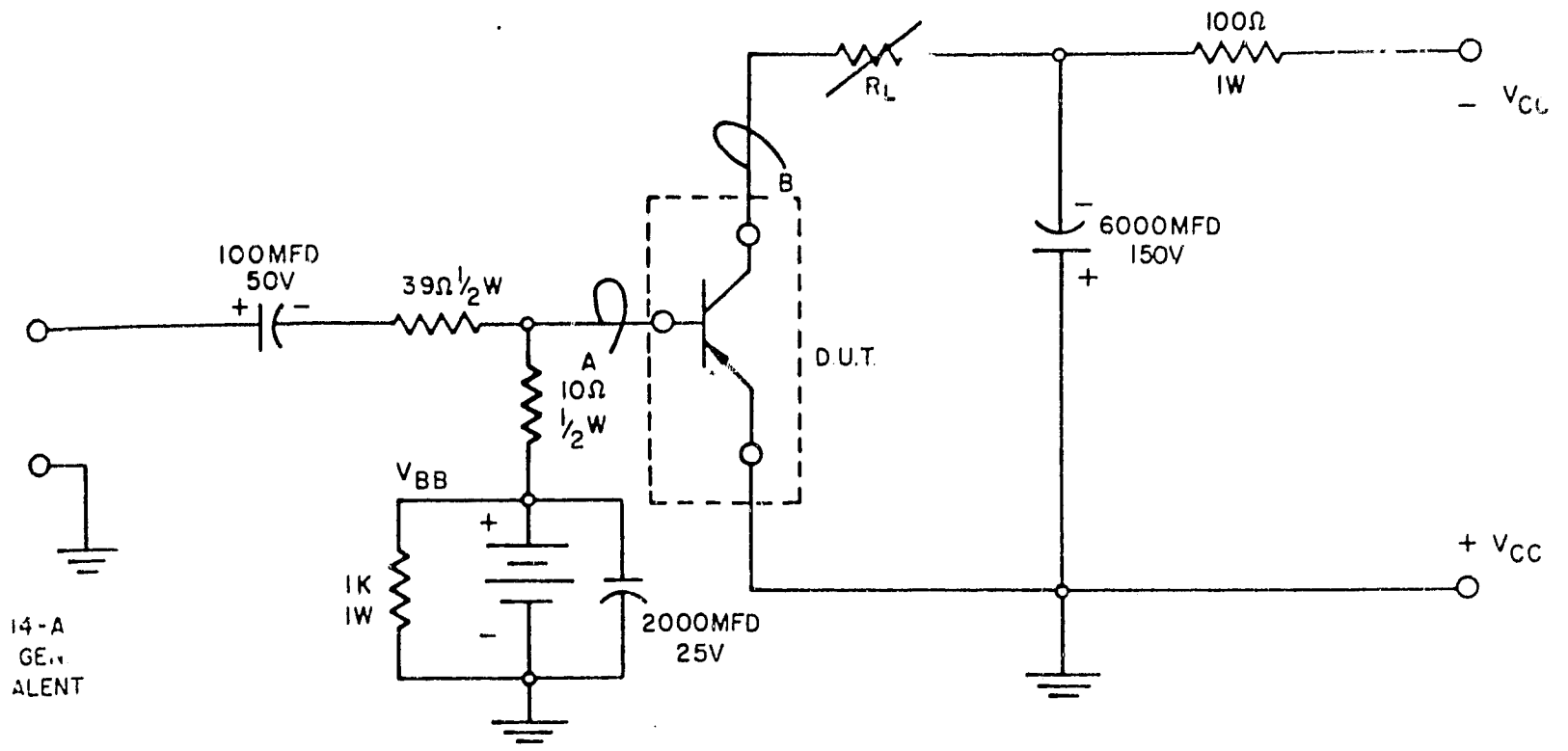
A special switching time circuit has been designed and constructed. It is shown schematically in Figure 6 .

B. ELECTRICAL RESULTS

During the course of this study, transistors with various physical parameters were fabricated and evaluated. Table 2 summarizes the electrical and physical parameters of three transistors that were used for evaluation of progress. Table 2 shows the physical parameters of the five final samples. Table 3a shows the voltage characteristics; Table 3b, the gain and saturation behavior; and Table 3c, the dynamics characteristics.

C. DISCUSSION

The purpose of this study was to develop a 100-ampere, 150-volt (sustaining), fast switching epitaxial base PNP power transistor with a gain of 15 and a $V_{CE(sat)}$ of 1 volt at I_C = 100 amperes. Early efforts showed that the W_B would have to be greater than the $\sim$2.5 microns used in the previous study to fabricate the 150-volt, 30-ampere PNP transistors. Initial results demonstrated that a 4 to 5 micron W_B would be needed to



V_{CC} = 150 V MAX.

I_{B_1} I_{B_2} = MEASURED AT POINT A WITH TEKTRONIX TYPE 131 PROBE

I_C = MEASURED AT POINT B WITH PEARSON TYPE 110 PROBE

R_L = ADJUST FOR SPECIFIED CURRENT AND VOLTAGE

Figure 6. Schematic - Switching Time Tester

Table 2

PHYSICAL PARAMETERS, FINAL SAMPLES

Run No.	Crystal No.	P^- X_j μ	ρ ohm-cm	N X_j μ	ρ ohm-cm	N^+ X_j μ	ρ ohm-cm	Emitter ρ atom/cc	X_j μ	W_B μ
C-995	611184	23	7.3	5.6	1	.3	.01	$5x10^{19}$	2.1	4.5
C-1006	611184	22	22	4.9	1	.3	.01	$5x10^{19}$	2.1	4.2
C-1004	611184	25	>100	5.2	1	.3	.01	$5x10^{19}$	2.7	4.8

Table 3a

ELECTRICAL EVALUATION, FINAL SAMPLES

100-AMPERE PNP TRANSISTORS

Parameter	V_{CBO}	I_{CBO}	V_{CEO}	I_{CEO}	V_{EBO}	I_{EBO}	$V_{CEO(sus)}$ I_C = 200mA
Units	volts	mA	volts	mA	volts	ma	volts
Unit No.							
C-1004C-1	50	1	50	1	4	80	185
C-1004C-3	50	5	50	8	4	50	230
C-995B-1	50	8	50	12	4	25	85
C-995B-1A	50	25	50	120	4	10	70
C-1006-2	50	11	50	11	4	3	165

Table 3b

Test Conditions	I_C =	1	10	20	40	60	80	100	Amperes
	(V_{CE} = 10V)								
Parameter		h_{FE}	h_{FE}	h_{FE}	h_{FE}	h_{FE}	h_{FE}	h_{FE}	
Unit No.									
C-1004C-1		20	30	25	20	18	12	10	
C-1004C-3		30	40	38	31	24	20	16	
C-995B-1		35	40	37	28	25	24	20	
C-995B-1A		40	71	69	64	54	47	43	
C-1006-2		63	71	67	50	43	31	22	

Table 3b (cont'd.)

Test Conditions I_C =	1		20		40		60		80		100 Amperes	
Parameter	V_{CE}	V_{BE}	V_{CE}	V_{BE}	V_{CE}	V_{BE}	V_{CE}	V_{BE}	V_{CE}	V_{BE}	V_{CE}	$V_{BE(sat)}$
Units	V	V	V	V	V	V	V	V	V	V	V	V
Unit No.												
C-1004C-1	.05	.7	.7	1.4	1.4	2.2	2.2	2.7	3.5	4.0	4.5	5.0
C-1004C-3	.05	.76	.9	1.7	2.0	2.4	1.9	3.4	3.5	4.2	4.0	4.6
C-995B-1	.02	.56	.12	.8	.4	1.0	.6	1.3	1.0	1.6	1.2	4.9
C-995B-1A	.01	.58	.15	.98	.2	1.0	.5	1.4	.8	1.7	1.0	2.0
C-1006-2	.05	.68	.25	1.0	.7	1.4	1.0	1.8	1.7	2.2	2.4	2.6

Table 3c

	Frequency Response			Saturated Switching
Test Conditions	V_{CC} = 30V; I_C = 20A; I_B = 4A			V_{CC} = 10V; I_C = 2A
Parameter	t_r	t_s	t_r	f_t
Units	μs	μs	μs	MHz
Unit No.				
C-1004C-1	.41	.65	.16	8.0
C-1004C-1	.40	.64	.18	9.5
C-995B-1	.37	.80	.36	9.8
C-995B-1A	.37	.88	.6	8.5
C-1006-2	.42	.82	.38	12.0

produce 150-volt, 100-ampere transistors. The dependence of $V_{CEO(sus)}$ on device area, for a given base width, is usually attributed to variations in epitaxial growth and diffusion and to the crystal defects that influence these variations. Efforts were concentrated on relatively wide base widths to insure acceptable voltages while investigating techniques to improve gain and saturation performance.

The most effective method of increasing lifetime was a P_2O_5 gettering operation after the emitter diffusion, as previously discussed.

The final samples are from three different epitaxial runs. Their physical parameters are similar except for the collector resistivity. C-995B-1 and B-1A have the lowest collector resistivity, the lowest $V_{CEO(sus)}$ and $V_{CE(sat)}$ and the highest h_{FE}. C-1004C-1 and -3 have the highest $V_{CEO(sus)}$ and $V_{CE(sat)}$ and the lowest h_{FE}. C-1006-2 falls between the others in gain, saturation and sustaining voltages.

Even though the base width is wider than the value for the previous 30-ampere study, the saturated switching times and frequency response are good for such a large area device. Since it is known that secondary breakdown protection generally increases with increasing W_B, it is expected that these transistors are stronger than devices with a 2.5 micron W_B.

5. CONCLUSIONS AND RECOMMENDATIONS

None of the five final samples meet all of the design objective specifications. C-995B-1 meets the gain and saturation specifications but not $V_{CEO(sus)}$. C-1006-2 exceeds the $V_{CEO(sus)}$ and h_{FE} requirements but not those for $V_{CE(sat)}$ or $V_{BE(sat)}$. C-1004C-1 exceeds the $V_{CEO(sus)}$ specifications but not those for gain or saturation. However the results reported demonstrate an advance in the state-of-the-art for fast switching, Si PNP power transistors. A single chip PNP transistor, large enough to handle 100 amperes and having sustaining voltages above 200V represents an advance in the state-of-the-art. This was made possible by the inherent advantage of the epitaxial base technique over other fast switching transistor processes which generally involve a base diffusion.

Improvements in the gain and saturation performance of a $150V_{(sus)}$, 100A PNP transistor will come from improvements in processing. Techniques to further improve crystal lifetime would result in improved device characteristics.

Although the relation of physical parameters to electrical characteristics has been determined, the affect of crystal or process induced defects has not been investigated.

Improved physical parameters resulting from more nearly perfect crystal and/or fewer process induced defects should permit narrower base widths to improve gain and saturation performance while retaining the desired voltage.